DK_USB2.0_GW2AR-LV18QN88PC7I6_GW1NSR-LV4CMG64PC7I6_V3.0

User Guide

DBUG408-1.0.4E, 05/09/2025

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Revision History

Date	Version	Description
07/15/2022	1.0E	Initial version published.
11/02/2023	1.0.1E	“Figure 2-4 System Block Diagram” in “2 Development Board Introduction” updated.
11/10/2023	1.0.2E	“Figure 3-5 Connection Diagram of LED” in “3.7 LED Module” updated.
02/02/2024	1.0.3E	The description of “2.1 Overview” optimized.
05/09/2025	1.0.4E	The caption for “Figure 2-2 A Development Board Kit” updated.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

DK_USB2.0_GW2AR-LV18QN88PC8I7_GW1NSR-LV4CMG64PC7I6_V3.0 development board (hereinafter referred to development board) user guide consists of following three parts:

1. A brief introduction to the features of the development board;
2. An introduction to the development board system architecture and hardware resources;
3. An introduction to the functions, circuits, and pinouts of each module.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS226, GW2AR series of FPGA Products Data Sheet
2. UG115, GW2AR-18 Pinout
3. UG229, GW2AR series of FPGA Products Package and Pinout User Guide
4. DS861, GW1NSR series of FPGA Products Data Sheet
5. UG864, GW1NSR-4 Pinout
6. UG863, GW1NSR series of FPGA Products Package and Pinout User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double-Data-Rate Synchronous Dynamic Random Access Memory
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable I/O
LDO	Low Dropout Regulator
LUT4	4-input Look-up Table
LVDS	Low-Voltage Differential Signaling
SSRAM	Shadow Static Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

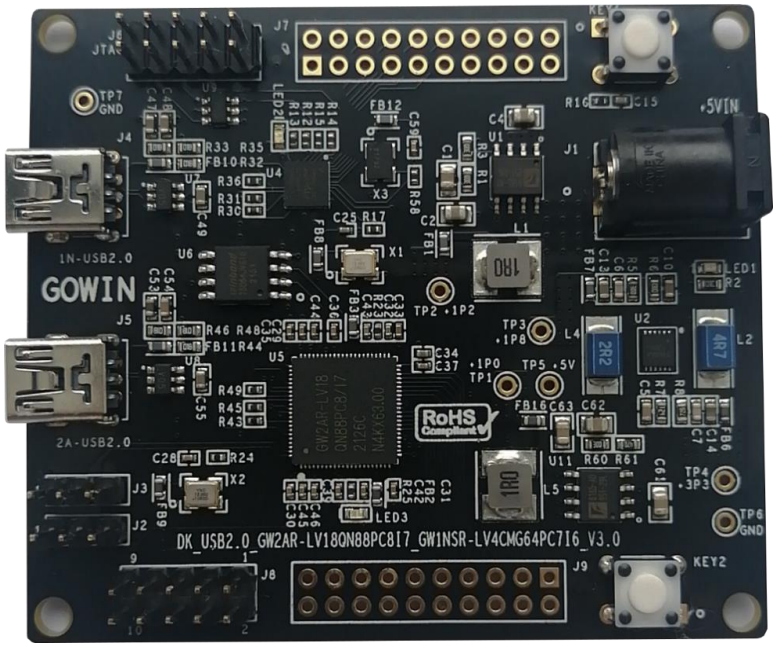
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_USB2.0_GW2AR-LV18QN88PC8I7_GW1NSR-LV4CMG64PC7I6_V3.0 Development Board



DK_USB2.0_GW2AR-LV18QN88PC8I7_GW1NSR-LV4CMG64PC7I6_V3.0 development board can apply to USB 2.0 communication, USB communication test, the function evaluation of GW1NSR-4C and GW2AR-18 series of FPGA, hardware reliability verification, and software learning and debugging.

The development board uses Gowin GW2AR-LV18QN88P FPGA products, which are the first generation products of the Arora family. As a kind of SIP chips, GW2AR series of FPGA products offer a range of features and rich resources like high-performance DSP, high-speed LVDS interface and abundant BSRAM resources. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make

the GW2AR series of FPGA products ideal for high-speed and low-cost applications.

The development board uses Gowin GW1NSR-LV4CMG64P FPGA products, which are the first generation products of the LittleBee family. As a kind of SIP chips, GW1NSR-LV4MG64P chip integrates GW1NS series of FPGA products and PSRAM chips.

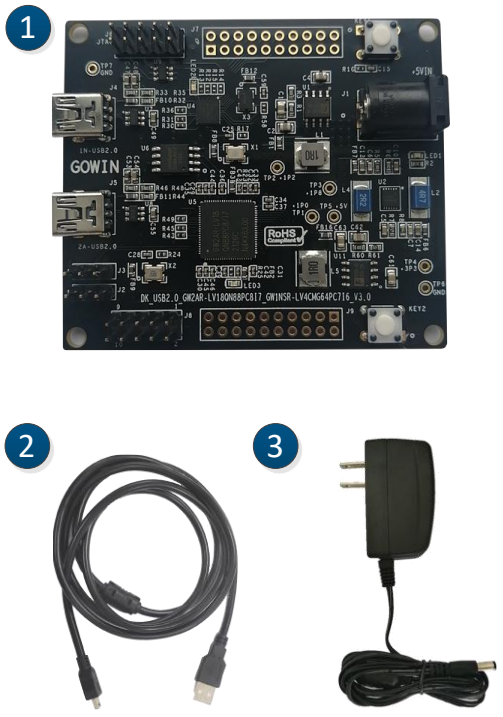
The development board supports 480Mbps high-speed (HS) and 12Mbps full-speed (FS) USB communication; the GW2AR-LV18QN88P is externally connected to FLASH chip to store the FPGA configuration program; keys and LEDs are convenient for user debugging.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_USB2.0_GW2AR-LV18QN88PC8I7_GW1NSR-LV4CMG64PC7I6_V3.0 development board
2. 5V power (input: AC 100-240V~50/60Hz 25VA, output: DC 5V 2A)
3. USB Mini B Cable

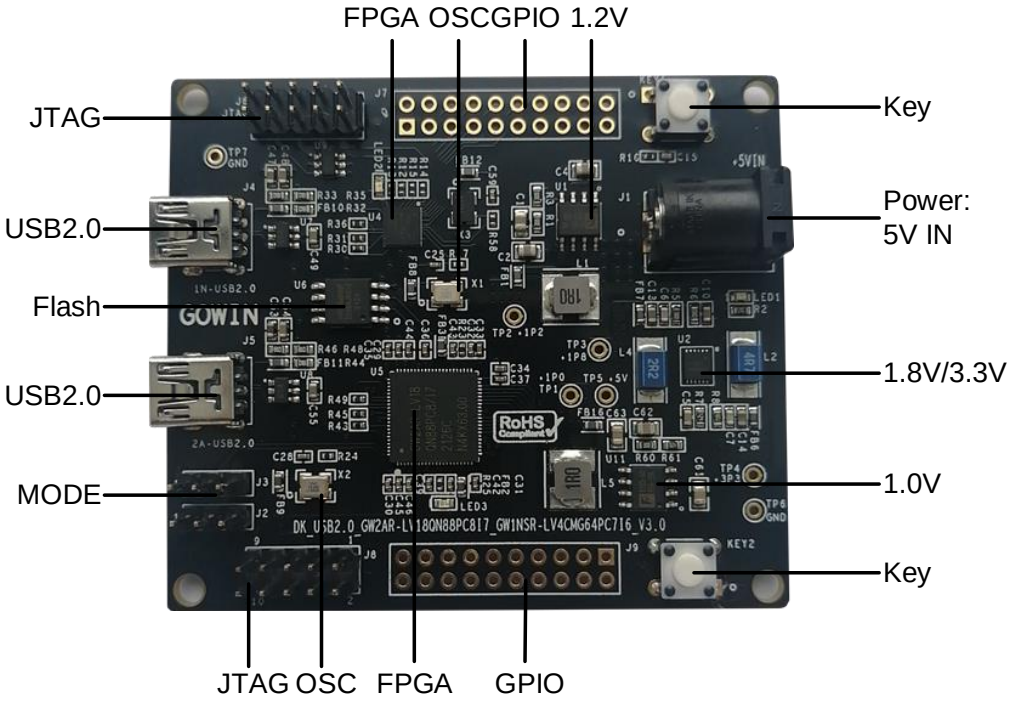
Figure 2-2 A Development Board Kit



① DK_USB2.0_GW2AR-LV18QN88PC8I7_GW1NSR-LV4CMG64PC7I6_V3.0 development board
② USB Mini B data cable
③ 5V power (Input: 100-240V~50/60Hz 0.5A, Output: DC 5V 2A)

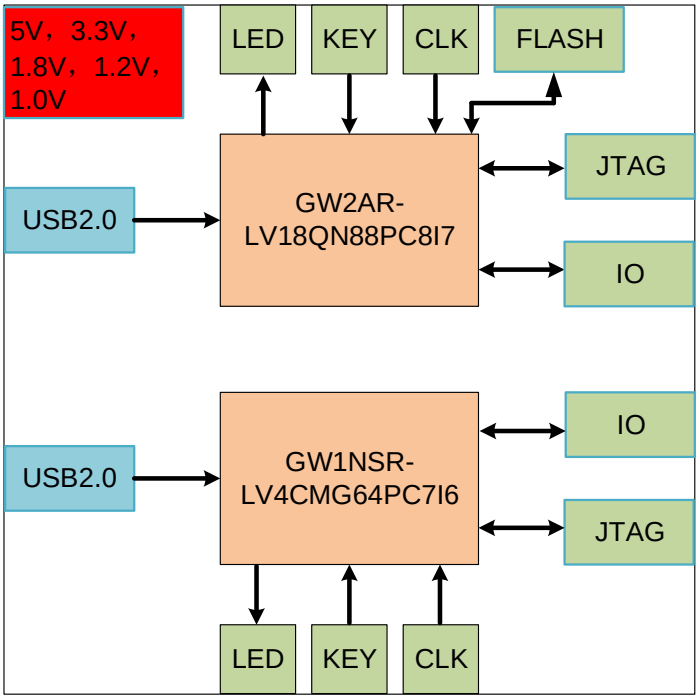
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

1. The FPGA device
   - Gowin GW2AR-LV18QN88P, GW1NSR-LV4CMG64P
   - Max. user I/O: 66, 55
2. Download and Boot
   - Integrate download module on the board, download through JTAG cable
   - Flash boot
   - After loading, boot board.
3. Power
   - External DC 5V 2A
   - The green POWER light is on after power on
   - The development board generates 5V, 3.3V, 1.8V, 1.2V, 1.0V, and 1.0V
4. Clock system

   12MHz crystal oscillator input
5. Memory Device

   64Mbit FLASH
6. USB 2.0 interface
   - One USB 2.0 interface communicates with GW2AR-LV18QN88P
   - One USB 2.0 interface communicates with GW1NSR-LV4CMG64P
7. GPIO Interface

   GPIO interface, enable communication with peripherals.
8. Debug
   - Two keys
   - Two green LEDs

Note!
Each FPGA chip connects to one key and one LED.

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW2AR FPGA products, please refer to *DS226, GW2AR Series of FPGA Products*.

For the resources of GW1NSR FPGA products, please refer to *DS861, GW1NSR Series of FPGA Products*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG229, GW2AR Series of FPGA Products Package and Pinout User Guide* for more details.

For the I/O BANK, package, and pinout information, see *UG863, GW1NSR Series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Download Module

3.2.1 Introduction

The development board provides a JTAG download interface. You can set the MODE value to download the programs to the on-chip SRAM or external Flash. When downloaded to SRAM, the bitstream file will be lost if the device is power down. When downloaded to Flash, the bitstream file will not be lost if the device powers down.

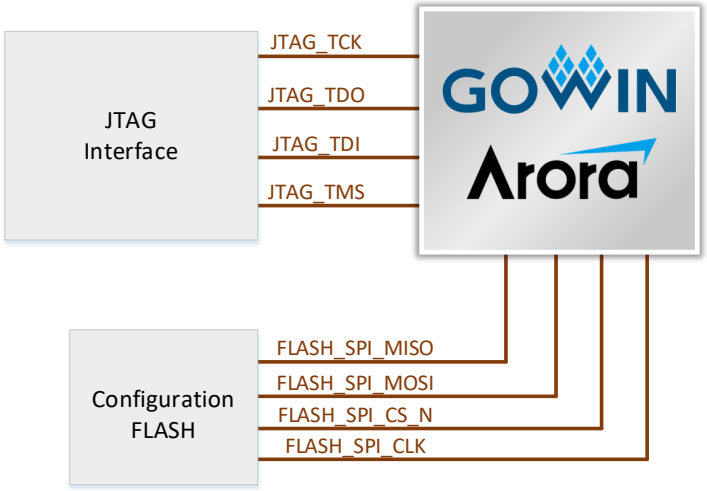
The MODE value configuration is as follows:

1. In any mode, you can download the bitstream file to the on-chip SRAM and run it immediately.

2. Set MODE as "011" to download the bitstream file to the external Flash. Set MODE to "000" and power on again. The device will read the FPGA configuration data from the Flash automatically.

The connection diagram of download and configuration is as shown in Figure 3-1.

Figure 3-1 Connection Diagram of FPGA Download and Configuration



3.2.2 Pinout

Table 3-1 FPGA-GW2AR-LV18QN88P Download and Configuration Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F2_TCK	6	2	1.8V	JTAG Signal
F2_TDO	8	2	1.8V	JTAG Signal
F2_TDI	7	2	1.8V	JTAG Signal
F2_TMS	5	2	1.8V	JTAG Signal
MSPI_DO	62	3	3.3V	Configure FLASH Signal
MSPI_DI	61	3	3.3V	Configure FLASH Signal
MSPI_CS	60	3	3.3V	Configure FLASH Signal
MSPI_CK	59	3	3.3V	Configure FLASH Signal

Table 3-2 FPGA-GW1NSR-LV4CMG64P Download and Configuration Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F1_TCK	D3	0	3.3V	JTAG Signal
F1_TDO	E3	0	3.3V	JTAG Signal
F1_TDI	E2	0	3.3V	JTAG Signal
F1_TMS	D2	0	3.3V	JTAG Signal

3.3 Power Supply

3.3.1 Introduction

The development board is powered via a power adapter. The input parameter is 100-240V~50/60MHz 25VA, and the output is DC +5V 2A.

The input 5V power can generate 3.3V, 1.8V, 1.2V, and 1.0V via the power supply chip on the development board.

- Use two FP6165ADXR-G1 power chips to generate 1.2V and 1.0V power, and the maximum output current is 3A.
- Use one PAM2306AYPAA DC-DC power chip to generate 3.3V and 1.8V power, and the maximum output current is 1A.

3.4 Clock and Reset

3.4.1 Introduction

The development board offers a 12MHz oscillator connecting to the global clock pins and 8.192MHz IIS clock for FPGA-GW1NSR-LV4CMG64P at the same time.

The development board offers a 12MHz oscillator connecting to the global clock pins and 8.192MHz IIS clock for FPGA-GW2AR-LV18QN88P at the same time.

The development board resets through the key, and press the key to reset FPGA after power up.

Figure 3-2 Connection Diagram of Clock and Reset

3.4.2 Pinout

Table 3-3 GW1NSR-LV4CMG64P Clock and Reset Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F1_CLK	C5	1	3.3V	12MHz crystal oscillator input
F1_IIS_CLK	C4	1	3.3V	8.192MHz
F1_RST_N	A5	1	3.3V	Reset Signal, active Low

Table 3-4 GW2AR-LV18QN88P Clock and Reset Pinout

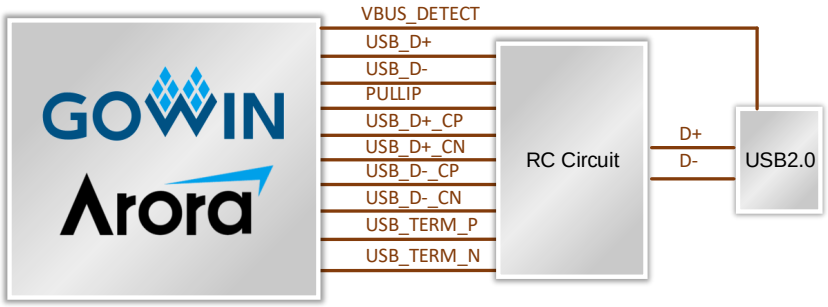
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F2_CLK	10	6	3.3V/2.5V	12MHz crystal oscillator input
F2_IIS_CLK	35	4	3.3V	8.192MHz
F2_RST_N	19	6	3.3V/2.5V	Reset Signal, active-low

3.5 USB 2.0 interface

3.5.1 Introduction

USB 2.0 interface is directly connected to FPGA through configuration resistor. The connection diagram is as shown in Figure 3-3.

Figure 3-3 Connection Diagram of FPGA and USB 2.0 Interface



3.5.2 Pinout

Table 3-5 GW1NSR-LV4CMG64P USB 2.0 Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1N_Pullip	G6	2	3.3V	Pull-up
USB_1N_D+_CP	G7	2	3.3V	USB+ signal
USB_1N_D+/-_CN	H7	2	3.3V	USB+ Reference signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_1N_D-_CP	G3	2	3.3V	USB- signal
USB_1N_D+/-_CN	H3	2	3.3V	USB- Reference signal
1N_Term_p	G5	2	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
1N_Term_n	H5	2	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
USB_1N_D+	G4	2	3.3V	USB high speed data pin
USB_1N_D-	H4	2	3.3V	USB high speed data pin
VBUS_DETECT_1N	G2	2	3.3V	VBUS disconnect detection to reset USB

Table 3-6 GW2AR-LV18QN88P USB 2.0 Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
2A_Pullip	80	0	3.3V	Pull-up
USB_2A_D+_CP	77	1	3.3V	USB+ signal
USB_2A_D+/-_CN	76	1	3.3V	USB+ Reference signal
USB_2A_D-_CP	71	1	3.3V	USB- signal
USB_2A_D+/-_CN	70	1	3.3V	USB- Reference signal
2A_Term_p	75	1	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
2A_Term_n	74	1	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
USB_2A_D+	73	1	3.3V	USB high speed data pin
USB_2A_D-	72	1	3.3V	USB high speed data pin
VBUS_DETECT_2A	83	0	3.3V	VBUS disconnect detection to reset USB

3.6 GPIO

3.6.1 Introduction

There are 40 GPIOs reserved on the development board, including eight 3.3V pins, four ground pins, fourteen GW1NSR-LV4CMG64P pins, and fourteen GW2AR-LV18QN88P pins. The connection diagram is as shown in Figure 3-4.

Figure 3-4 Connection Diagram of GPIO

3.6.2 Pinout

Table 3-7 GW1NSR-LV4CMG64P GPIO Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1N_GPIO0	A1	1	3.3V	GPIO0
1N_GPIO1	B1	1	3.3V	GPIO1
1N_GPIO2	A2	1	3.3V	GPIO2
1N_GPIO3	B2	1	3.3V	GPIO3
1N_GPIO4	B3	1	3.3V	GPIO4
1N_GPIO5	A3	1	3.3V	GPIO5
1N_GPIO6	B4	1	3.3V	GPIO6
1N_GPIO7	A4	1	3.3V	GPIO7
1N_GPIO8	B6	1	3.3V	GPIO8
1N_GPIO9	A6	1	3.3V	GPIO9
1N_GPIO10	B7	1	3.3V	GPIO10
1N_GPIO11	A7	1	3.3V	GPIO11
1N_GPIO12	A8	1	3.3V	GPIO12
1N_GPIO13	B8	1	3.3V	GPIO13

Table 3-8 GW2AR-LV18QN88P GPIO Pinout

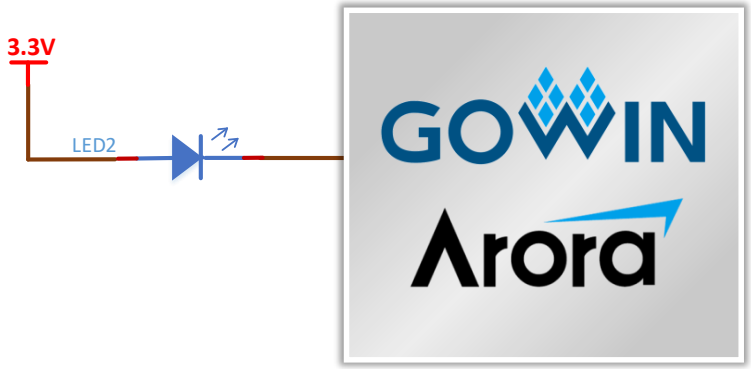
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
2A_GPIO0	42	4	3.3V	GPIO0
2A_GPIO1	41	4	3.3V	GPIO1
2A_GPIO2	40	4	3.3V	GPIO2
2A_GPIO3	39	4	3.3V	GPIO3
2A_GPIO4	38	4	3.3V	GPIO4
2A_GPIO5	37	4	3.3V	GPIO5
2A_GPIO6	33	5	3.3V	GPIO6
2A_GPIO7	32	5	3.3V	GPIO7
2A_GPIO8	31	5	3.3V	GPIO8
2A_GPIO9	30	5	3.3V	GPIO9
2A_GPIO10	29	5	3.3V	GPIO10
2A_GPIO11	26	5	3.3V	GPIO11
2A_GPIO12	27	5	3.3V	GPIO12
2A_GPIO13	28	5	3.3V	GPIO13

3.7 LED Module

3.7.1 Introduction

Two green LEDs on the development board and are used to display the required status. When the output signal of FPGA corresponding pin is low, the LED is lit up. When the output signal is high, the LED is off. The connection diagram is as shown in Figure 3-5.

Figure 3-5 Connection Diagram of LED



3.7.2 Pinout

Table 3-9 GW1NSR-LV4CMG64P LED Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F1_LED	G1	2	3.3V	LED 1

Table 3-10 GW2AR-LV18QN88P LED Pinout

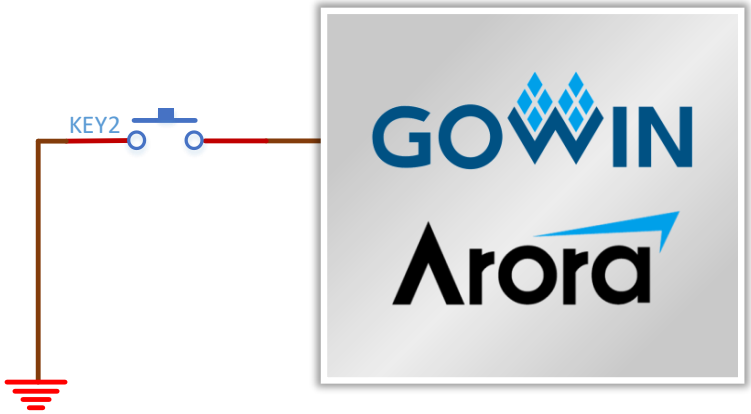
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F2_LED	13	6	3.3V	LED 2

3.8 Keys Module

3.8.1 Introduction

The development board has two keys that can be used to control input during testing. When the key is pressed, the input is low. The connection diagram is as shown in Figure 3-6.

Figure 3-6 Key Circuit



3.8.2 Pinout

Table 3-11 GW1NSR-LV4CMG64P Keys Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F1_RST_N	A5	1	3.3V	KEY1

Table 3-12 GW2AR-LV18QN88P Key Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F2_RST_N	19	6	3.3V/2.5V	KEY2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